UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,810	09/25/2003	Michael J. Hennessy	HENN-2	7751

7590 04/05/2006

LEONARD COOPER
999 GRANT AVENUE
PELHAM MANOR, NY 10803

EXAMINER	
KAPLAN, HAL IRA	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,810	HENNESSY ET AL.	
	Examiner	Art Unit	
	Hal I. Kaplan	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: Page 7, line 9 contains the phrase "V(2,con)". It appears this should read "V(2,on)".

Appropriate correction is required.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 16 in Figure 2 (see page 5, line 25); 40 in Figure 10 (see page 7, lines 28-30); and 30 and 40 in Figure 11 (see page 7, lines 28-30). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1, 11, and 14 objected to because of the following informalities: Claim 1, line 3 contains the phrase "losses;". It appears this should read "losses; and". Claims 11 and 14, line 2 contains the phrase "first module, to switch off". It appears this should

read "first module, and to switch off". Claims 11 and 14, line 3 contains the phrase "load current said control circuit". It appears this should read "load current, said control circuit". Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 8, 10, 11, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by the US patent of Bowles (5,155,289).

As to claim 1, Bowles, drawn to high-voltage solid-state switching devices, teaches, in Figures 6 and 7B, a hybrid switch, comprising: a first switching module (607B,611B) for switching voltages and currents and incurring switching losses (see column 8, lines 20-29 and column 8, line 64 through column 9, line 32); and a second switching module (606B,609B) for conducting current and incurring conduction losses (see column 8, lines 20-29 and column 8, line 64 through column 9, line 32); said first and second modules (606B,607B,609B,611B) being connected electrically in parallel, and respectively controllable to be in one of an open non-conducting state and a closed conducting state, at least one said module having solid state construction (see column 8, line 64 through column 9, line 32 and Figure 7B).

As to claim 2, at least one of the modules (606B,609B) includes a MOSFET (609B) (see column 8, line 65).

As to claim 3, the first module (607B,611B) is chosen from the group consisting of IGBTs, IGCTs, thyristors, and diodes (see column 8, lines 64-65).

As to claims 4 and 13, the hybrid switch of Bowles further comprises a control circuit for switching the first module (607B,611B) and the second module (606B,609B) on and off in a predetermined sequence and for predetermined intervals (see column 9, line 41 through column 10, line 26; column 13, lines 63-65; and Figure 9C).

As to claim 8, at least two second modules (606B,609B) used for conducting currents are connected in series (see column 8, lines 65-67; column 17, lines 46-52; and Figure 7B).

As to claim 10, at least two first modules (607B,611B) used for switching voltages and currents are connected in series (see column 8, lines 67-78; column 17, lines 46-52; and Figure 7B).

As to claims 11 and 14, the control circuit operates the modules (606B,607B,609B,611B) to pass load current through the second module (606B,609B) while bypassing the first module (607B,611B), and to switch off the load current, the control circuit turns the second module (606B,609B) off to divert the load current to the first module (607B,611B) and then turns the first module (607B,611B) to the off state (see column 12, lines 60 through column 13, line 20).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 5, 6, 12, and 15-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Bowles in view of the US patent of Gold et al. (5,953,224).

As to claims 5, 12, 15, and 18-20, Bowles teaches all of the claimed features, as set forth above, except for at least one of the first module and the second module being cryogenically cooled. Gold, drawn to a control circuit for cryogenically-cooled power electronics employed in power conversion systems, teaches, in Figures 1-3, cryogenically cooling a switching circuit (see column 2, line 60 through column 3, line 4,

and column 8, lines 28-42). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to cryogenically cool the switch of Bowles, as taught by Gold, in order to enhance its electrical characteristics.

As to claim 6, the control circuit (21) of Gold is cryogenically cooled (see column 2, lines 60-64 and column 10, lines 5-6).

As to claims 16 and 17, Gold teaches the use of a refrigeration unit (18) cryogenically cooling at least one module (see column 6, lines 36-39).

10. Claims 7 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bowles in view of the US patent of Vercelloti et al. (5,774,000).

As to claims 7 and 21, Bowles teaches all of the claimed features, as set forth above, except for at least two second modules used for conducting currents connected in parallel, and at least another two second modules used for conducting currents connected in series. Vercelloti, drawn to a DC semiconductor switch, teaches, in Figure 6, a hybrid switch comprising two switching modules (68,20), wherein at least two second modules (20_1,20_2) used for conducting currents are connected in parallel (see column 4, lines 45-50; column 6, lines 45-51; column 6, line 66 through column 7, line 2; and column 7, lines 25-36). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to build the switch of Bowles with two second modules connected in parallel, as taught by Vercelloti, in order to reduce the steady state power dissipation and provide backup in the event of failure of one of the second modules.

11. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bowles in view of the US patent of Yamaguchi (5,828,112).

As to claim 9, Bowles teaches all of the claimed features, as set forth above, except for at least two first modules used for switching voltages and currents connected in parallel. Yamaguchi, drawn to a semiconductor device incorporating an output element having a current-detecting section, teaches, in Figure 6, a hybrid switch comprising two switching modules (IGBT,DIODE,CURRENT DETECTING SECTION), wherein at least two first modules (IGBT,DIODE) used for switching voltages and currents are connected in parallel (see column 1, lines 52-57; column 8, lines 40-44; and Figure 6). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to build the switch of Bowles with two first modules connected in parallel, as taught by Yamaguchi, because it is conventional to design the switching circuit in this way.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal I. Kaplan whose telephone number is 571-272-8587. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

hik

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800